KWM-001

PATENT APPLICATION

REMARKS

This preliminary amendment is requested prior to the initial examination of the above-identified patent application to reduce multiple dependency claims to reduce the initial filing fee. Further, this preliminary amendment is requested to make number of words in the Abstract less than 150. No new matter has been introduced. Entry of this amendment is respectfully requested. Additionally, in accordance with 37 CFR 1.121(c))(1), amended abstract and claims are set forth in a marked-up version in the pages attached to this preliminary amendment. If the Examiner has any suggestions for placing this application in even better form, the Examiner is invited to telephone the undersigned and the number listed below.

Respectfully submitted,

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Appendix

In accordance with 37 CFR 1.121(b)(1)(iii), the amended claims and abstract are set forth in a marked-up version below:

IN THE CLAIMS:

6. The semiconductor device according to [any one of claims 1 to 5] claim 1 or 2, wherein a second metal layer made of said second metal or said third metal layer is provided on a right surface and a side surface of said bump electrode made of said first metal, so that said first and second semiconductor chips are joined to each other via said alloy layer or via said third metal layer.

7. The semiconductor device according to [any one of claims 1 to 6] claim 1 or 2 , said joining portion where said first and second semiconductor chips are joined to each other has such a fillet formed thereon that is made of an alloy layer of said first metal and said second metal or said third metal layer.

8. The semiconductor device according to claim 1, [4, 5, 6, or 7,] wherein said first metal is Au and said second metal is Sn, so that said joining portion has an Au-Sn alloy.

9. The semiconductor device according to claim 2, [4, 5, 6, or 7,] wherein said third metal is made of an Au-Sn alloy.

12. The semiconductor device according to claim 10 [or 11], further comprising:

a second insulating layer provided between said wiring and a passivation film on the surface of said semiconductor chip to flatten the surface of said wiring.

13. The semiconductor device according to [any one of claims 10 to 12] claim 10, wherein said wiring is made of an Au, which is provided so as to connect to said electrode terminal via a barrier metal layer, and

wherein said low-melting point metal layer is made of an Au-Sn alloy.

14. The semiconductor device according to [any one of claims 10 to 12] claim 10, wherein said wiring comprising:

a Cu wiring made of Cu formed simultaneously with said electrode terminal;

a barrier metal layer provided on said Cu wiring; and

an Au wiring provided on said barrier metal layer,

wherein said low-melting point metal layer is made of an Au-Sn alloy and is provided on said Au wire.

15. The semiconductor device according to [any one of claims 10 to 13] claim 10, wherein said wiring is made of Au formed simultaneously with said electrode terminal, and said low-melting point metal layer is made of an Au-Sn alloy.

16. The semiconductor device according to claim [7, 8, 12, 13, 14, or 15] 8 or 9, wherein said Au-Sn alloy constituting said joining portion has an Au-rich composition containing at least 65 weight-percent of Au.

17. The semiconductor device according to claim [7, 8, 12, 13, 14, 15, or 16] claim 8 or 9, wherein an Au-Sn alloy layer of said joining portion has a thickness of 0.8 μ m or more and 5 μ m or less.

18. The semiconductor device according to [any one of claims 1 to 10] claim 1 or 2, further comprising:

an insulating resin layer provided at a gap between said first and second semiconductor chips joined each other to fill the gap, said insulating resin layer having nearly the same elastic modulus as said bump electrode.

19. The semiconductor device according to [any one of claims 1 to 10] claim 1 or 2, further comprising:

an insulating resin layer having a thermal shrinkage factor of 5% or less, which is provided at a gap between said first and second semiconductor chips joined each other to fill the gap.

20. The semiconductor device according to [any one of claims 1 to 19] claim 1, wherein a circuit element is formed in a semiconductor layer at said joining portion of at least one of said first and second semiconductor chips.

24. The method according to claim [21, 22, or 23] 21 or 22, further comprising the steps of:

alloying said metals provided on the surface of said electrode terminal or said wiring of one of said first and second semiconductor chips with said low-melting point metal layer

provided on the surface thereof; and

joining to the other of said first and second semiconductor chips or substrate.

IN THE ABSTRACT:

In a [disclosed] COC type semiconductor device, a bump electrode [(21)] of a second semiconductor chip [(2)] is joined to a first semiconductor chip [(1)] having a bump electrode [(11)] formed thereon. The bump electrodes [(11)] and [(21)] of the respective first and second semiconductor chips [(1)] and [(2)] are both made of first metal such as Au having a relatively high melting point, while a joining portion of these bump electrodes [(11)] and [(21)] is formed of an alloy layer [(3)] of the first metal and second metal, which second metal is made of such a material that can melt at a lower temperature than the melting point of the first metal to be alloyed with it. As a result, in the COC type semiconductor device, when interconnecting a plurality of semiconductor chips, their electrode terminals can be joined to each other without deteriorating the properties of these chips owing to the high temperature applied thereon.